EK6709

Rev. 1.0

DATA SHEET

TFT LCD Timing Controller

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fitipower integrated technology Inc.

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TFT LCD Timing Controller

1. GENERAL DESCRIPTION

The EK6709 is a TFT LCD timing controller. It resides on the flat panel display and provides the interface signal and timing control between graphics and a TFT-LCD system.

The EK6709 chip links the panel's system interface to the display via the input data bus. The data is then routed to the source and gate display drivers.

2. FEATURES

- Wide supply voltage: 2.7V to 3.6V
- 6 bit data single port input and single port output
- Support up/down and Left/Right image rotation
- Support 3 display resolutions that are 640×480, 800×480 and 800×600
- Support both DE and Sync mode
- Support Flicker Free Technology
- Build-in Self Test mode
- Built-in Power on Reset
- Green-64 pin TQFP

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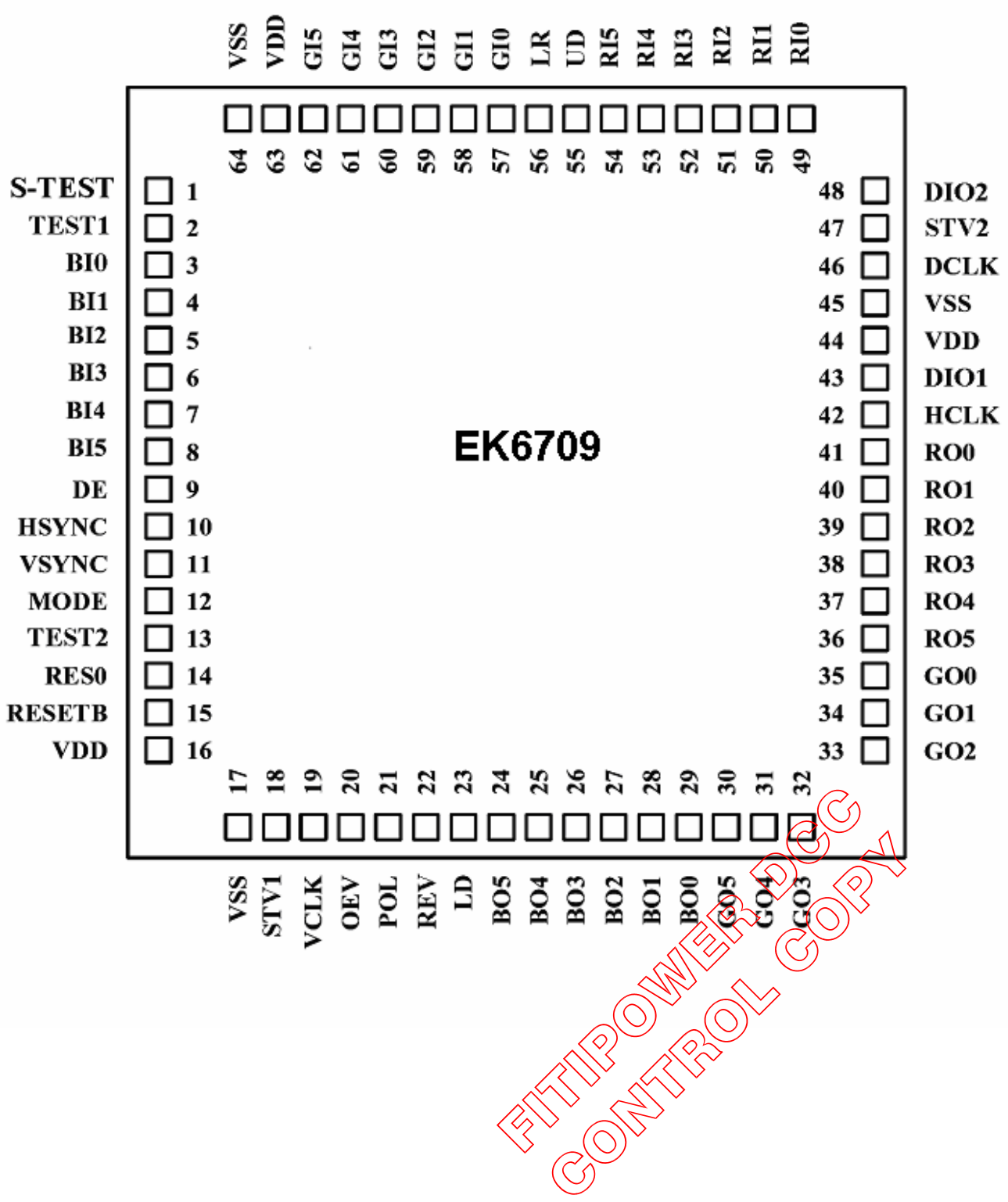
3. PIN ASSIGNMENT



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4. PIN DESCRIPTION

Pin Name	Pin No.	Pin Type	Description
DCLK	46	Input	Clock signal; latching data at the falling edge.
RI5-RI0 GI5-GI0 BI5-BI0	54-49 62-57 8-3	Input	Data input. 6-bit data.
DE	9	Input	Data enable signal.
HSYNC	10	Input	Horizontal sync input. Negative polarity.
VSYNC	11	Input	Vertical sync input. Negative polarity.
MODE	12	Input	DE / HV MODE select. Normally pulled high. 1: DE mode, 0: HV mode.
RES0	14	Input	Resolution Selection 1: 800×480 and 800×600 0: 640×480
RESETB	15	Input	Reset pin, active low. Normally pulled high.
STV1, STV2	18, 47	Output	Gate Start Pulse.
VCLK	19	Output	Gate driver shift clock.
OEV	20	Output	Gate output off signal.
POL	21	Output	Polarity invert signal of Source Driver IC.
REV	22	Output	Data polarity invert control signal output.
LD	23	Output	Latch Pulse of Source Driver IC.
RO5-RO0 GO5-GO0 BO5-BO0	36-41 30-35 24-29	Output	Data Output
HCLK	42	Output	Source driver shift clock.
DIO1, DIO2	43, 48	Output	Source Start Pulse.
UD	55	Input	UD = 1 | STV1 Output | STV2 Tristate UD = 0 | STV2 Output | STV1 Tristate
LR	56	Input	LR = 1 | DIO1 Output | DIO2 Tristate LR = 0 | DIO2 Output | DIO1 Tristate
TEST1, TEST2	2, 13	Input	Please pull high in normal operation.
S_TEST (pull low)	1	Input	0 = Normal operation 1 = Self Test Mode enable
VDD	16, 44, 63	Power	Power supply for digital circuits.
VSS	17, 45 64	Power	Ground pins for digital circuits.

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5. INPUT TIMING

800x600 and 800x480

SYNC MODE	800 × 600/480			
Parameter	Min	Typ	Max	Unit
Clock Freq.	32	40	43	MHZ
H-sync Total	850	1056	1100	CLK
H-sync Pluse Width	1	1	1	CLK
H-sync Pluse Width + Back Porch	46	46	46	CLK
H-sync Front proch	4	210	254	CLK
H- Active	800	800	800	CLK
V-sync Total	628	635	650	LINE
V-sync Pluse Width	1	1	1	LINE
V-sync Pluse Width + Back Porch	23	23	23	LINE
V-sync Front proch	5	12	27	LINE
V- Active	600	600	600	LINE
DE MODE	**800 × 600/480**			
H-sync Total	850	1056	1100	CLK
H- Active	800	800	800	CLK
H- Blanking	50	256	300	CLK
V-sync Total	628	500	550	LINE
V- Active	600	600	600	LINE
V- Blanking	28	35	50	LINE

640x480

SYNC MODE	640 × 480			
Parameter	Min	Typ	Max	Unit
Clock Freq.	23	25	30	MHZ
H-sync Total	750	800	900	CLK
H-sync Pluse Width	1	1	1	CLK
H-sync Pluse Width + Back Porch	46	46	46	CLK
H-sync Front proch	64	114	214	CLK
H- Active	640	640	640	CLK
V-sync Total	515	525	560	LINE
V-sync Pluse Width	1	1	1	LINE
V-sync Pluse Width+Back Porch	34	34	34	LINE
V-sync Front proch	1	11	46	LINE
V- Active	480	480	480	LINE
DE MODE	**640 × 480**			
H-sync Total	750	800	900	CLK
H- Active	640	640	640	CLK
H- Blanking	110	160	260	CLK
V-sync Total	515	525	560	LINE
V- Active	480	480	480	LINE
V- Blanking	35	45	80	LINE

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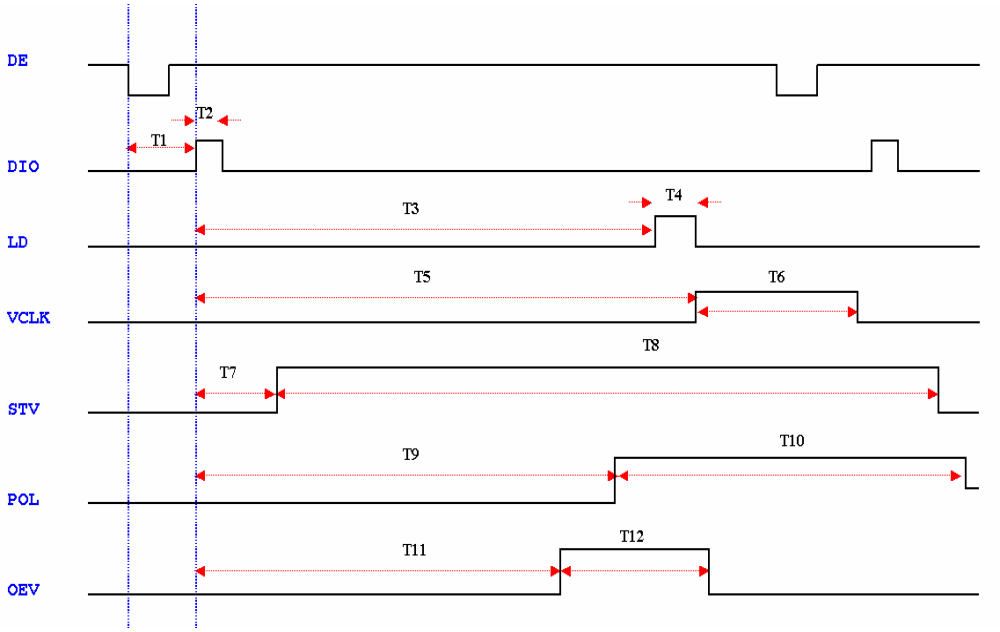
6. OUTPUT TIMING



	Symbol	640 × 480	800 × 480 800 × 600	Unit
DE-rising to DIO rising	T1	TBD	TBD	CLK
DIO high duration	T2	1	1	CLK
DIO rising to LD rising	T3	493	813	CLK
LD high duration	T4	4	4	CLK
DIO-rising to VCLK rising	T5	497	817	CLK
VCLK high duration	T6	238	398	CLK
DIO rising to STV rising	T7	9	9	CLK
STV high duration	T8	580	898	CLK
DIO rising to POL rising	T9	650	805	CLK
POL high duration	T10	1L	1L	LINE
DIO rising to OEV rising	T11	571	709	CLK
OEV high duration	T12	96	120	CLK

7. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3 to +4.6	V
Input Voltage	VI	-0.3 and VI+0.3	V
Output Voltage	VO	-0.3 and VI+0.3	V
Storage temperature	Tstg	-55 to +125	Deg. C
Operation temperature	Top	-25 to +85	Deg. C
Junction temperature	Tj	+150	Deg. C

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

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8. DC ELECTRICAL CHARACTERISTICS

(Input/Output level / VSS= 0V, VDD = 3.0~3.6V, TA = –25~85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level Input voltage	V_{IH}	CMOS	0.7VDD	-	-	V
Low level Input voltage	V_{IL}	CMOS	-	-	0.2VDD	V
High level Input voltage	V_{IH}	RESET Pin	0.75VDD	-	-	V
Low level Input voltage	V_{IL}	RESET Pin	-	-	0.15VDD	V
High level Output voltage	V_{OH}	I_{OH} = –8mA	VDD – 0.8	-	-	V
Low level Output voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Input leakage current	I_{IL}	V_I = VDD, VSS	–10	-	+10	uA
Output leakage current	I_{OZ}	Hiz – output	–10	-	+10	uA
Pull up resistance	R_{UP}	-	50	100	200	k ohm
Pull down resistance	R_{DN}	-	50	100	200	k ohm

9. AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fdclk	5	-	50	MHZ
DCLK	Tduty	-	-	-	-
DCLK period	Tcp	20	-	-	ns
DCLK High time	Tch	0.3	-	-	Tcp
DCLK Low time	Tcl	0.3	-	-	Tcp
RGB Input Data Setup time	Tids	5	-	-	ns
RGB Input Data Hold time	Tidh	10	-	-	ns
DE Setup time	Tdes	5	-	-	ns
DE Hold time	Tdeh	10	-	-	ns
HSYNC Setup time	Thss	5	-	-	ns
HSYNC Hold time	Thsh	10	-	-	ns
VSYNC Setup time	Tvss	5	-	-	ns
VSYNC Hold time	Tvsh	10	-	-	ns
VSYNC↓ to HSYNC↓ Delay	Tvh	0	-	-	ns
Data hold time	Tsu	8	-	-	ns
Data set-up time	Thd	4	-	-	ns
HCLK pulse width	Tcw	3	-	-	ns

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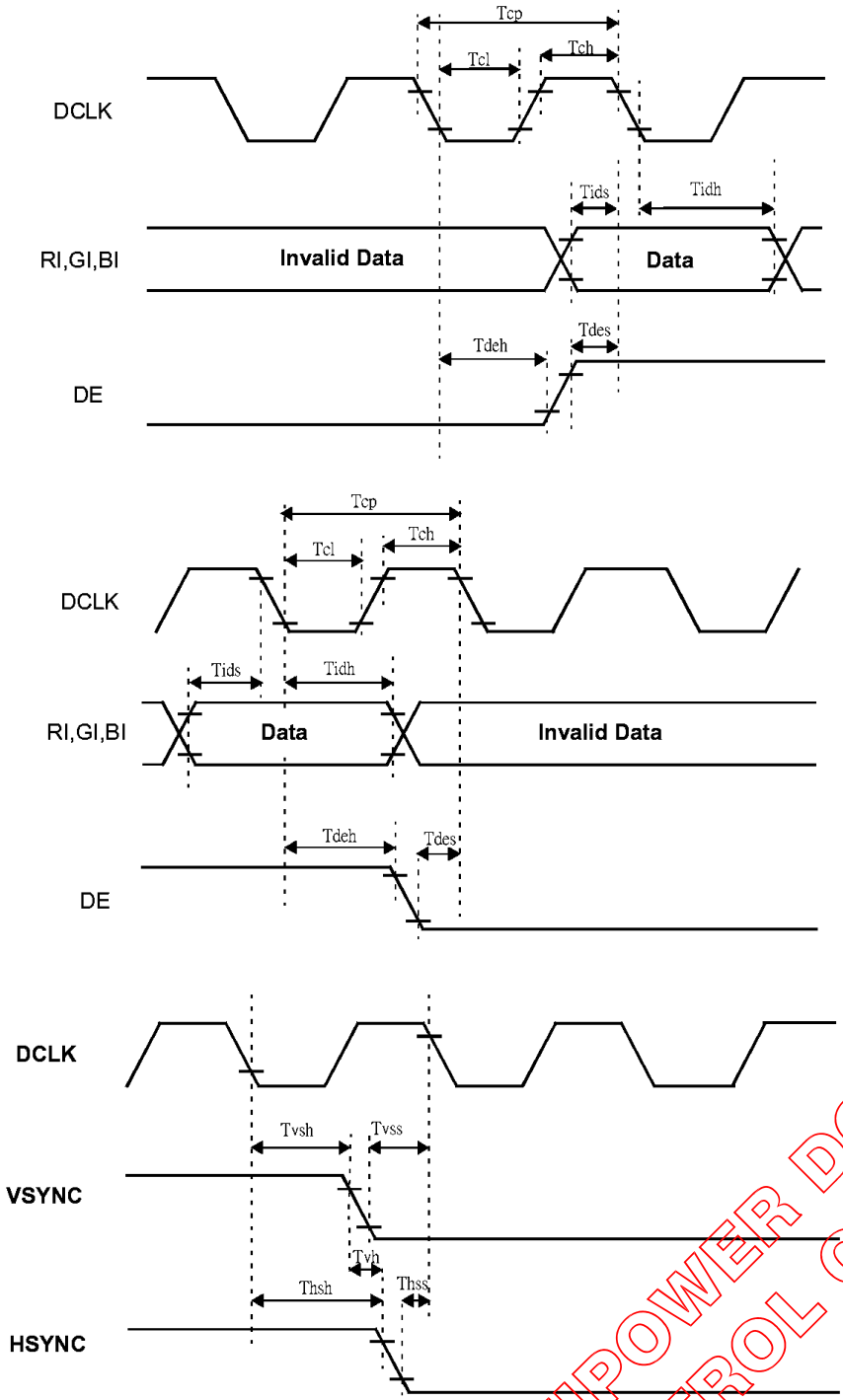
Input Signal Timing Chart



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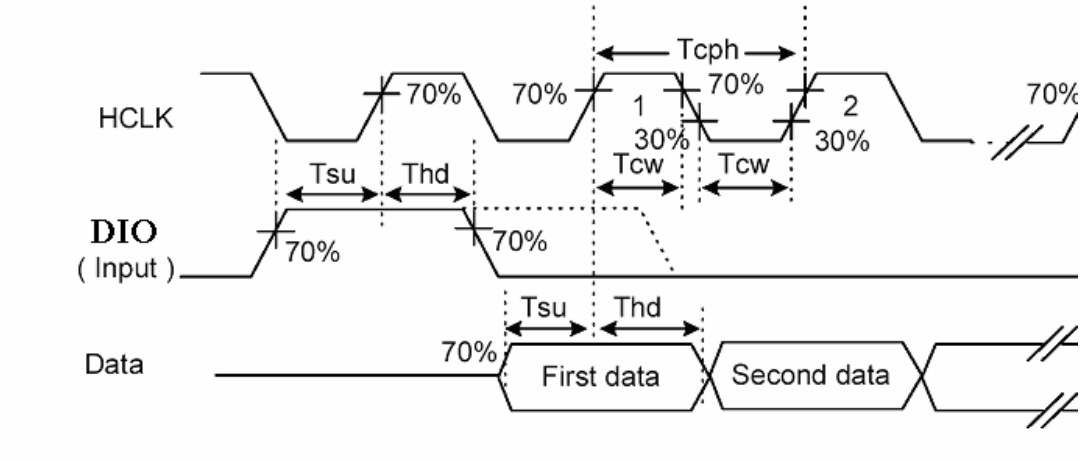
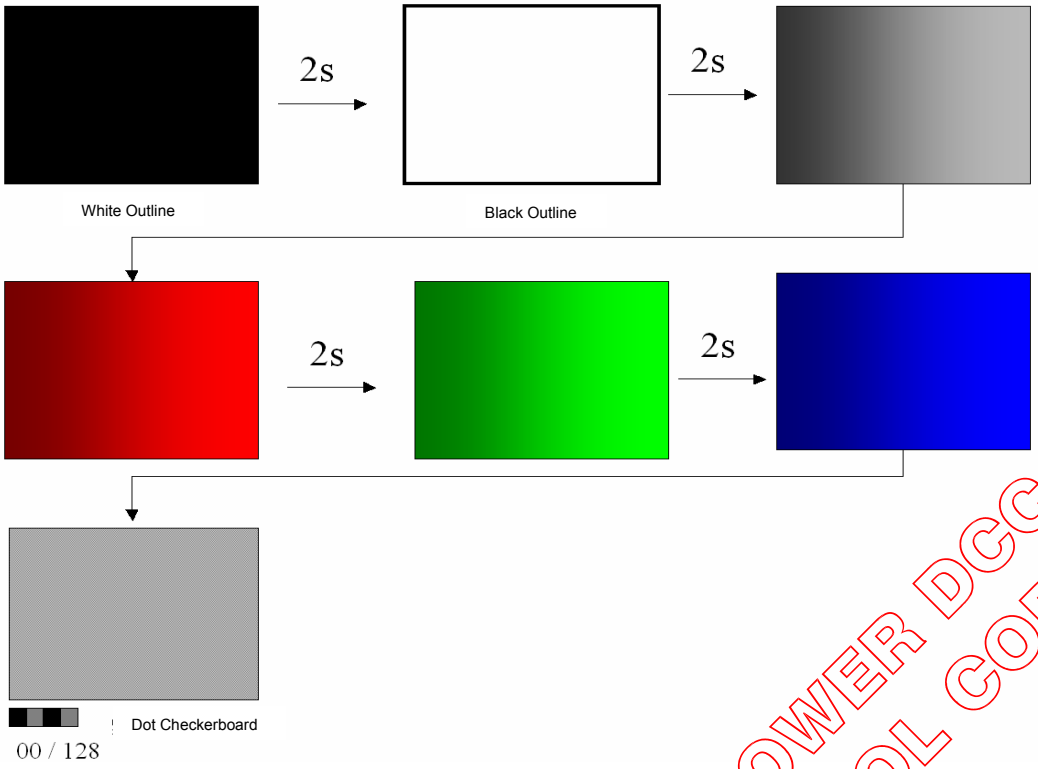
Output Signal Timing Chart



10. SELF TEST PATTERN

Note: The display has related to Mode [1:0]. The input clock rate use typical definition.



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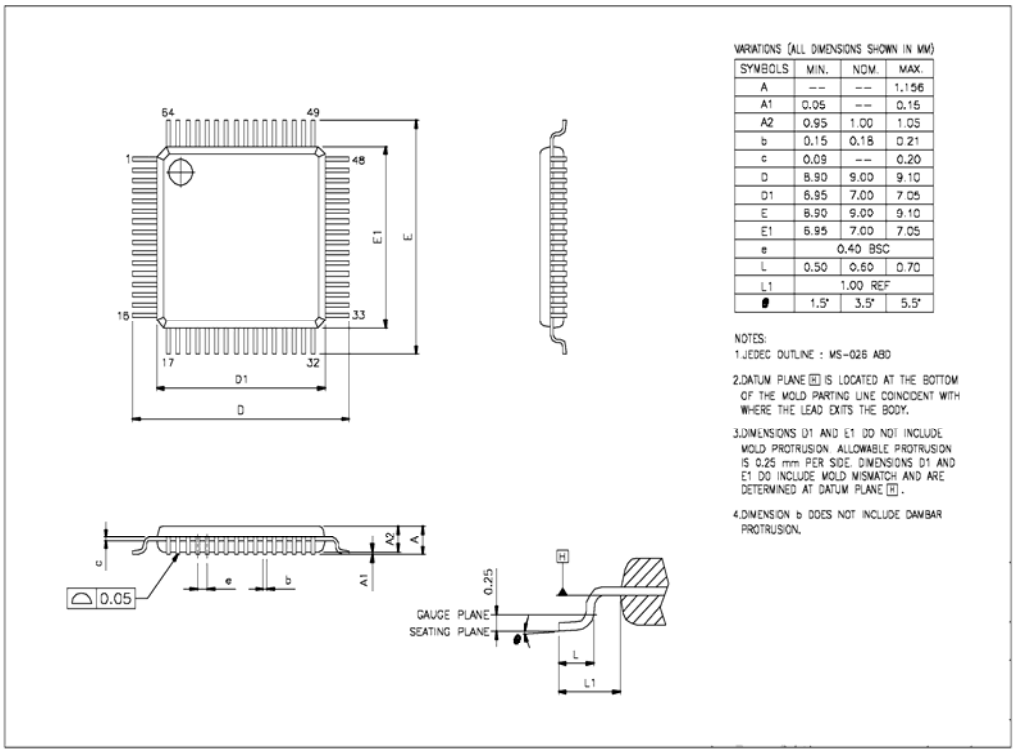
11. PACKAGE INFORMATION

7 × 7mm TQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.156
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.15	0.18	0.21
c	0.09	--	0.20
D	8.90	9.00	9.10
D1	6.95	7.00	7.05
E	8.90	9.00	9.10
E1	6.95	7.00	7.05
e	0.40 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
θ	1.5°	3.5°	5.5°

NOTES:
1.JEDEC OUTLINE : MS-026 ABD

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

12. REVISION HISTORY

1.0

- ✧ New issue

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